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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,928	03/31/2001	John T. Orchard	15685P096	7550

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EXAMINER	
NGO, CHUONG D	
ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/823,928	ORCHARD, JOHN T.	
	Examiner	Art Unit	
	Chuong D. Ngo	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4-17 and 19-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4-17 and 19-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2,4-17, and 19-31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Grisamore (6,535,901) in view of Yamazaki et al. (7,706,211).

As per claims 2,11,12,14-17,26,27 and 29-31, Grisamore discloses in figures 5 a method for implementing a Wallace-architecture in which input terms are analyzed on a bit-wise basis (see the bridging paragraph of cols. 4 and 5, where each level of bit significance is a column of bit) to segment each level of bit significance of input terms into one or more-groups of three bits (circled three dots), and/or one or more groups of two bits (circled two dot and/or one or more group of one bit (non-circled dots). Full-adders (3-dot circle) and half adders (2-dot circle) are selected to perform Boolean functions on 3-bit groups and 2-bit groups, respectively. The number of adders are clearly depend on a bit-wise analysis of the input terms within each level of bit-significance as claimed (see the bridging paragraph of cols. 4 and 5). Grisamore also discloses in figures 1 a multi-input adder (18) as claimed. It is noted that Grisamore does not teach registers in figure 5. However, Grisamore discloses in col.1, lines 33-40 that it is known in the art to use registers at optimal points in a multiplier to enable pipelined processing which provides a high through put multiply accumulate circuit. Further Yamazaki et al. disclosed in figure 2 and 5 a multiplier having register placed at optimal point in the multiplier for enabling pipeline processing to multiply data at a high data rate (see col.1, lines 13-42). Thus it would have been obvious to a person of ordinary skill in the art to provides the Wallace-architecture of Grisamore with registers at optimal points in the architecture to enable pipelined processing in

order to increase the through put of circuit and to process data at a high data rate. The memory 16 in figure 1 would have been thus a part of pipelined registers.

As per claims 4,13,19-25 and 28, since it is well know in the art to implement a multiplier by a FPGA (see the cited references), it would have been obvious to a person of ordinary skill in the art, as a matter of design choice, to implement the multiplier by a FPGA as claimed.

2. Claims 2,4-17 and 19-31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Costa et al. (5,935,201) in view of Yamazaki et al. (7,706,211.

As per claims 2,11,12,14-17,26,27 and 29-31, Costa et al. discloses in figures 7-9 a Wallace-architecture in which full-adders (3-input block) and half adders (2-input block) are selected to perform Boolean functions respectively on 3-bit groups and 2-bit groups in each level of bit significance of input terms (each adder in figures 7 and 8 is labeled corresponding to the levels of bit significance of input terms) . The numbers of adders are clearly depend on a bit-wise analysis of the input terms within each level of bit-significance. Groups of one bit are corresponding to the input terms that are not input to an adder in figures 7 and 8. Costa also discloses in figures 9 a multi-input adder (16 BITS LOOKAHEAD ADDER) as claimed. It is noted that Costa et al does not teach registers in the Wallace-architecture. However, since it is known in the art to use registers at optimal points in a multiplier to enable pipelined processing which provides a high through put multiply circuit as disclosed Yamazaki et al. in figure 2 and 5 which show multipliers having register placed at optimal point in the multiplier for enabling pipeline processing to multiply data at a high data rate (see col.1, lines 13-42), it would have been obvious to a person of ordinary skill in the art to provides the Wallace-architecture of Costa

et al. with registers at optimal points in the architecture to enable pipelined processing in order increase the through put of circuit and to process data at a high data rate. The (PIPNINE REG. N 1(16 BITS) in figure 9 would have been thus a part of pipelined registers .

As per claims 4,13,19-25 and 28, since it is well know in the art to implement a multiplier by a FPGA (see the cited references), it would have been obvious to a person of ordinary skill in the art, as a matter of design choice, to implement the multiplier by a FPGA as claimed.

3. Applicant's arguments filed on 01/03/2007 have been fully considered but they are not persuasive because the memory 16 and adder 18 of Grisamore, and the PIPNINE REG. N 1(16 BITS) and the 16 BITS LOOKAHEAD ADDER of Costa can be seen as a part of Wallace-architecture since the are connected together.

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong D. Ngo whose telephone number is (571) 272-3731. The examiner can normally be reached on Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong D Ngo
Primary Examiner
Art Unit 2193

04/14/2007